METAL GATE STRUCTURE FOR MOS DEVICES

BACKGROUND

[0001] The present invention relates generally to integrated circuit (IC) designs, and more particularly to a metal oxide semiconductor (MOS) device with a metal gate and a cap layer.

[0002] Conventionally, the gate conductor of a semiconductor device, such as a complementary metal-oxide-semiconductor (CMOS) transistor, is made of polycrystalline silicon doped with either N-type or P-type impurities. While such doped impurities reduce the resistance of the poly-silicon gate conductor, they have undesired electrical characteristics. The doped poly-silicon gate conductor would induce an undesired depletion region thereunder in a substrate. As the size of a semiconductor device keeps shrinking, this undesired depletion region may significantly hinder the improvement of its performance. Thus, it is desirable to replace the conventional poly-silicon gate conductor with other materials that do not require impurity doping, in order to avoid this depletion problem.

[0003] Another challenge facing the poly-silicon gate is its low quality electrical interface with a metal contact. To meet this challenge, a silicide layer is formed atop the poly-silicon gate conductor as its interface with the metal contact to reduce resistance thereacross. The silicide layer can be formed by a series of process steps, called self-aligned silicide (salicide) technology, that eliminates a photolithography step, and provides a near perfect alignment for the silicide layer and the poly-silicon gate conductor. This is a significant advantage because, otherwise, the photolithography step will impose a dimension limit on designs of semiconductor device, due to its pattern resolution. Needless to say, the photolithography step costs extra overhead.

[0004] Given the superiority of the self-aligned process, it is also desirable to form a self-aligned contact atop a source/drain region. However, the salicide technology for the poly-silicon gate conductor is often not compatible with the process steps for forming the self-aligned contact. When forming the self-aligned contact, a metal layer is deposited over the source/drain regions, thermally treated, and then etched back. In order to avoid an undesired electrical connection between the gate conductor and the source/drain regions through the self-aligned contact, a cap layer is usually formed atop the gate conductor as a protection layer. Because of this cap layer, the salicide layer and the self-aligned contact cannot be formed in the same process steps.

[0005] What is needed is MOS device with a gate structure of a non-ploy-silicon material, which eliminates the need of a salicide layer, such that the self-aligned contact may be implemented in a simplified fabrication process.

SUMMARY

[0006] The present invention discloses a gate structure for MOS devices. In one embodiment, the gate structure includes a gate dielectric layer disposed on a semiconductor substrate, a metal gate conductor disposed on the gate dielectric layer, a cap layer disposed on the metal gate conductor, at least one spacer covering sidewalls of the metal gate conductor and the cap layer, such that the cap layer and the spacer encloses the metal gate conductor layer therein, and at least one self-aligned contact structure formed next to the metal gate conductor on the semiconductor substrate. As such, the cap layer and the spacer separate the self-aligned contact structure from directly contacting the metal gate conductor.

[0007] The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] **FIGS. 1A-1B** illustrate a conventional MOS device with a metal gate conductor.

[0009] **FIGS. 2A-2B** illustrate a conventional MOS device with a poly-silicon gate conductor.

[0010] **FIGS. 3A-3B** illustrate a MOS device with a metal gate conductor, a cap layer, and a self-aligned contact structure, in accordance with one embodiment of the present invention.

[0011] **FIGS. 4A-4B** illustrate a MOS device with a metal gate conductor, a cap layer, and a self-aligned contact structure, in accordance with another embodiment of the present invention.

[0012] **FIG. 5** illustrates a process flow for fabricating the above-mentioned MOS device, in accordance with one embodiment of the present invention.

DESCRIPTION

[0013] **FIG. 1A** illustrates a cross section of a conventional MOS device **100** on a semiconductor substrate **102**. A method to successfully from at least one conductive plug adjacent to at least one metal gate conductor will be discussed in detail below. Shallow trench isolations (STIs) **104** first define an active area therebetween. A gate dielectric layer **106** is formed atop the substrate **102**, and covered by a metal gate conductor **108**. A low doped drain **110** is formed. The gate structure, which includes the gate dielectric layer **106** and the metal gate conductor **108**, is covered on their sidewalls by spacers **112**. Plus-doped source/drain regions **114** are formed. A salicide source/drain contact **116** is formed. An inter-level dielectric layer **118** is deposited over the metal gate conductor **108** and the sour/drain regions **114**. A contact via is etched in the inter-level dielectric layer **118**, down to the silicide layer **116**, and then filled with a conductive material to form a conductive plug **120**. A metal layer is then deposited and pattern-etched to form a metal interconnect **122**. Electrical connection is made from the metal interconnect **122**, through the plug **120**, to the salicide source/drain contact **116**.

[0014] **FIG. 1B** illustrates a cross section of a conventional MOS device **124**, which is the same as the MOS device **100** in **FIG. 1A**, except that two conductive plugs **126** are misaligned. The conductive plug **126** on the left is in contact with the salicide source/drain contact **116**, the sidewall spacers **112**, and the top surface of the metal gate conductor **108**. As a result, the salicide source/drain contact **116** and the metal gate conductor **108** are electrically connected. Due to this misalignment, the circuit will be shorted, thereby causing failure.